

CLAIMS

We claim:

1. A method for forming an integrated circuit device including a resistor  
5 pattern having a desired resistance value, comprising:  
forming a low resistive layer on an integrated circuit substrate;  
forming an insulating layer on the low resistive layer opposite the integrated  
circuit substrate; and  
forming a high resistive layer, having a specific resistance higher than the low  
10 resistive layer and of at least about a hundred  $\mu\Omega\cdot\text{cm}$ , on the insulating layer opposite  
the low resistive layer, wherein the low resistive layer, the insulating layer and the  
high resistive layer define the resistor pattern in a region of the integrated circuit  
substrate.
- 15 2. The method of Claim 1 wherein the integrated circuit device is an  
integrated circuit memory device including a capacitor and wherein the step of  
forming a low resistive layer comprises concurrently forming the low resistive layer  
defining the resistor pattern in the region of the integrated circuit substrate and  
forming an upper capacitor electrode of the capacitor in a different region of the  
20 integrated circuit substrate, wherein the low resistive layer defining the resistor pattern  
and the upper capacitor electrode are formed of the same material.
3. The method of Claim 2 wherein the low resistive layer comprises at  
least one of ruthenium (Ru), platinum (Pt), ruthenium oxide ( $\text{RuO}_2$ ), iridium (Ir),  
25 iridium oxide ( $\text{IrO}_2$ ), tungsten (W), aluminum (Al), copper (Cu), titanium nitride  
(TiN), tantalum nitride (TaN) and/or tungsten nitride (WN) and wherein the high  
resistive layer comprises a doped polysilicon.
4. The method of Claim 3 wherein the insulating layer comprises at least  
30 one of  $\text{SiO}_2$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{Al}_2\text{O}_3$  and/or  $\text{Si}_3\text{N}_4$ .
5. The method of Claim 3 further comprising forming at least one of a  
source and/or a drain in a cell region of the integrated circuit memory device between

the region of the integrated circuit substrate including the resistor pattern and the different region of the integrated circuit substrate including the capacitor.

6. The method of Claim 3 further comprising:

5 forming a first metal contact, having a first depth, to the upper capacitor electrode; and

forming a second metal contact, having a second depth different from the first depth, to the high resistive layer of the resistor pattern.

10 7. The method of Claim 3 further comprising forming a titanium nitride (TiN) layer between the low resistive layer and the insulating layer.

8. A method for forming an integrated circuit device including a resistor pattern having a desired resistance value, comprising:

15 forming a low resistive layer defining an upper capacitor electrode in a first region of an integrated circuit substrate and a low resistive layer of the resistor pattern in a second region of the integrated circuit substrate displaced from the first region;

forming an insulating layer on the upper capacitor electrode and on the low resistive layer of the resistor pattern opposite the integrated circuit substrate;

20 forming a high resistive layer on the insulating layer on the upper capacitor electrode and on the low resistive layer of the resistor pattern opposite the low resistive layer; and

wherein the low resistive layer, the insulating layer and the high resistive layer are formed through a single photolithography process using a single mask.

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9. The method of Claim 8 wherein the high resistive layer has a specific resistance of at least about a hundred  $\mu\Omega\cdot\text{cm}$ .

10. The method of Claim 9 further comprising forming a metal contact to  
30 the upper capacitor electrode and a metal contact to the high resistive layer of the resistor pattern using a two photomask process.

11. The method of Claim 10 wherein the integrated circuit device comprises an integrated circuit memory device having a junction region and wherein the two photo mask process further comprises forming a metal contact to the junction region.

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12. The method of Claim 9 wherein the steps of forming the low resistive layer, the insulating layer and the high resistive layer comprise:

depositing the low resistive layer over the entire surface of at least a portion of the integrated circuit substrate including the first region and the second region;

10 depositing the insulating layer on the low resistive layer;

depositing the high resistive layer on the insulating layer;

patterning the low resistive layer, the insulating layer and the high resistive layer to form the upper capacitor electrode in the first region and the resistor pattern in the second region of the integrated circuit substrate.

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13. The method of Claim 12 wherein the integrated circuit device comprises an integrated circuit memory device and wherein the first region comprises a cell region of the integrated circuit memory device and wherein the second region comprises a peripheral region of the integrated circuit memory device.

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14. A resistor pattern for an integrated circuit memory device having a capacitor, comprising:

an integrated circuit substrate;

25 a low resistive layer formed on the integrated circuit substrate, the low resistive layer defining an upper capacitor electrode of the capacitor and defining a low resistive layer of the resistor pattern in a region of the integrated circuit substrate displaced from the upper capacitor electrode;

an insulating layer formed on the upper capacitor electrode and the low resistive layer of the resistor pattern; and

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a high resistive layer formed on the insulating layer, the low resistive layer, the insulating layer and the high resistive layer defining the resistor pattern in the region of the integrated circuit substrate displaced from the upper capacitor electrode.

15. The resistor pattern of Claim 14 wherein the low resistive layer comprises a material having a specific resistance of at least a hundred  $\mu\Omega\cdot\text{cm}$ .

16. The resistor pattern of Claim 15 wherein the low resistive layer  
5 comprises at least one of Ru, Pt,  $\text{RuO}_2$ , Ir,  $\text{IrO}_2$ , W, Al, Cu, TiN, TaN, and/or WN.

17. The resistor pattern of Claim 14 wherein the insulating layer comprises at least one of  $\text{SiO}_2$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{Al}_2\text{O}_3$ , and/or  $\text{Si}_3\text{N}_4$ .

18. The resistor pattern of Claim 14 wherein the high resistive layer has a  
10 specific resistance of at least a hundred  $\mu\Omega\cdot\text{cm}$ .

19. The resistor pattern of Claim 18 wherein the high resistive layer has a specific resistance of at least a thousand  $\mu\Omega\cdot\text{cm}$ .

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20. The resistor pattern of Claim 18 wherein the high resistive layer comprises a doped polysilicon layer.

21. The resistor pattern of Claim 14 further comprising, a TiN layer  
20 formed between the low resistive layer and the insulating layer.

22. A method of forming a resistor pattern in a semiconductor memory device having a capacitor, the method comprising:

- 25 a) providing an integrated circuit substrate including a cell region and a periphery region, the cell region including a first cell region and a second cell region;
- b) depositing a low resistive material layer over all of a region of the semiconductor substrate including the cell region and the periphery region;
- c) depositing an insulating material layer on the low resistive material layer;
- d) depositing a high resistive material layer on the insulating layer; and
- 30 e) patterning the low resistive material layer, the insulating material layer and the high resistive material layer to form a low resistive layer, an insulating layer and a high resistive layer, respectively, over the first cell region and the periphery region of the integrated circuit substrate.

23. The method of Claim 22 wherein the low resistive material layer has a specific resistance of at least about a hundred  $\mu\Omega\cdot\text{cm}$ .

5           24. The method of Claim 23 wherein the low resistive material layer comprises at least one of Ru, Pt, RuO<sub>2</sub>, Ir, IrO<sub>2</sub>, W, Al, Cu, TiN, TaN, and/or WN.

25. The method of Claim 22 wherein the insulating material layer comprises at least one of SiO<sub>2</sub>, Ta<sub>2</sub>O<sub>5</sub>, Al<sub>2</sub>O<sub>3</sub>, and/or Si<sub>3</sub>N<sub>4</sub>.

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26. The method of Claim 22 wherein the high resistive material layer has a specific resistance of at least about a thousand  $\mu\Omega\cdot\text{cm}$ .

15           27. The method of Claim 26 wherein the high resistive material layer comprises a doped polysilicon layer.

28. The method of Claim 22 further comprising, after step (b), the step of depositing a TiN layer on the low resistive layer.

20           29. The method of Claim 22 further comprising, after step (a), the step of forming an under insulating layer on the entire surface of the integrated circuit substrate.

25           30. A method of forming metal contacts of a resistor pattern for use in an integrated circuit memory device having a capacitor, the method comprising:

          a) providing a integrated circuit substrate, the integrated circuit substrate including a cell region and a periphery region, the cell region including a first cell region and a second cell region, the first cell region including a first low resistive layer, a first insulating layer and a first high resistive layer that are sequentially  
30 stacked, the second cell region including a conductive layer, the periphery region including the resistor pattern, the resistor pattern including a second low resistive layer, a second insulating layer and a second high resistive layer that are sequentially stacked;

b) forming a planarization layer over all of a surface of the integrated circuit substrate in at least a region including the cell region and the periphery region; and

c) forming first to third metal contacts, the first metal contact formed in the first cell region and exposing a portion of the first low resistive layer, the second  
5 metal contact formed in the second cell region and exposing a portion of the conductive layer, the third metal contact formed in the periphery region and exposing a portion of the second high resistive layer.

31. The method of Claim 30 wherein step (c) includes forming the first  
10 metal contact using a first mask and forming the second metal contact and the third metal contact using a second mask.

32. The method of Claim 30 wherein step (c) includes forming the first  
metal contact and the second metal contact using a first mask and forming the third  
15 metal contact using a second mask.